

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P. O. Box 272400  
Fort Collins, Colorado 80527-2400



PATENT APPLICATION

ATTORNEY DOCKET NO. 200208051-1

IPe

IN THE  
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Benjamin T. Percer, et al.

Confirmation No.: TBA

Application No.: 10/606,463

Examiner: To Be Assigned

Filing Date: 06-26-2003

Group Art Unit: TBA

Title: Use of I2C-Based Potentiometers To Enable Voltage Rail Variation Under BMC Control

Commissioner for Patents

PO Box 1450

Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or  
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97 (c) together with either a:  
( ) Statement under 37 CFR 1.97(e), or  
( ) a \$180.00 fee under 37 CFR 1.17(p), or  
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:  
( ) Statement under 37 CFR 1.97(e)(1) or (2), and  
( ) a \$180.00 fee set forth in 37 CFR 1.17(p).  
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account 08-2025 the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

(X) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

( ) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: \_\_\_\_\_  
OR

Respectfully submitted,

Benjamin T. Percer, et al.

By \_\_\_\_\_

Michael G. Verga, Esq.

Attorney/Agent for Applicant(s)  
Reg. No. 39,410

Date: 12-09-2004

Telephone No.: (703) 591-2664

Typed Name: \_\_\_\_\_

Signature: \_\_\_\_\_



PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO. <b>200208051-1</b>	APPLICATION NO. <b>10/606,463</b>	CONFIRMATION NO. <b>TBA</b>
APPLICANT <b>Benjamin T. Percer, et al.</b>		
FILING DATE <b>06-26-2003</b>	GROUP <b>TBA</b>	

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
1A				
1B				
1C				
1D				
1E				
1F				
1G				
1H				
1I				
1J				
1K				

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
1L	GB 1 219 001	01-13-1971			
1M	JP 5-2502	01-08-1993			
1N					
1O					
1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

1Q	UK Search Report; Application No. GB0413501.8, November 5, 2004.
1R	Tsukude, et al. "Highly Reliable Testing of ULSI Memories with On-Chip Voltage-Down Converters". IEEE Design & Test Of Computers. June 1993, pgs. 6-12.
1S	Berner, et al. "DC Voltage Margin Tester.. NB84092465. IBM Technical Disclosure Bulletin, Vol. 27, No. 4B, September 1984, pg 246.

EXAMINER

DATE CONSIDERED